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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	PAPER NUMBER
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,253	YEH ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment received on 9/25/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed September 25th 2006. Claims 1-15 are pending. Applicant's arguments have been carefully and respectfully considered, but they are not entirely persuasive, as will be discussed in more detail below, even in light of the instant amendments. Accordingly, this action has been made FINAL.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by **Luo et al. (U.S Patent No. 6,169,700 hereafter referred to as Luo)**.

Independent Claims

With respect to **independent claim 1,**

> *"A multi-port memory system,* **[Luo discloses in the abstract, "dual port device"]** *comprising: a memory array with an addressable array of memory locations: at least two ports coupled to the memory array,* **[Luo discloses this**

limitation e.g. in the abstract, "An asynchronous wait state generator circuit and method is included in a dual port device, e.g., in a dual port memory, to allow the use of separate address decoders and simultaneous access to memory locations from asynchronously operating, separate ports. "] *each of the at least two ports transmitting to the memory array an address, a clock signal,* **["clock signal" disclosed in the abstract]** *and a read/write control signal;* **[Luo discloses in column 4, lines 4-8, "Conventional addressing, read/write and other control signals associated with the respective address and data buses are not shown for simplicity of explanation. "]** *and a collision detect circuit coupled to receive the address, the clock signal, and the read/write control signal from each of the at least two ports,* **[Luo discloses these limitations, e.g. in FIGs. 1-3 and associated text]** *wherein the collision detect circuit sets a collision flag* **["SAME_LOC"]** *when a collision condition is detected in any of the at least two ports, the collision flag providing an indication that any of the at least two ports may have read or written corrupted data."* **[Luo teaches this limitation, e.g. in column 4, lines 50-56, "If the two simultaneous addresses indicate a collision would occur in an access to the same address location, a same location signal SAME_LOC is activated, e.g., goes to a logic HIGH state for the duration of the collision of address signals. Otherwise, the same location signal SAME_LOC remains inactive, e.g., at a logic LOW state." Luo also discloses this limitation in column 6, line 67 – column 5, lines 1-5]**

With respect to **independent claim 8**,

"A dual port memory system, comprising: a memory array coupled to receive a left port memory address and a right port memory address; **[FIG. 1, elements "FROM ADDR 1, FROM ADDR 2, DATA 1, and DATA 2"]** *and a collision detect circuit* **[FIG. 1, elements 110, 120, and 123]** *configured to detect a match between the left port memory address and the right port memory address and generate a left port collision flag if the right port is writing data, and generate a right port collision flag if the left port is writing data, the collision flag providing an indication that one of the right port or the left port may have read or written corrupted data."* **[Luo discloses in column 4, lines 57-61, "The asynchronous, simultaneous access wait state generator 123 generates a wait state signal WAIT STATE 1 relating to the first port of the dual port device, and a wait state signal WAIT STATE 2 relating to access from the second port of the dual port device. "]**

With respect to **independent claim 11**, and **claim 12**,

"A method of collision detection in a dual port memory system, comprising: detecting that a left port address to be presented to a left port is identical to a right port address to be presented to a right port; and generating a left port collision flag if a write operation is being processed for the right port address at the right port, the collision flag providing an indication that the left port may have read or written corrupted data." **[Luo discloses in column 4, lines 57-61, "The asynchronous, simultaneous access wait state generator 123 generates a wait state signal WAIT STATE 1 relating to the first port of the dual port device, and a wait state signal WAIT STATE 2 relating to access from the second port of the dual port device. " Luo teaches this limitation, e.g. in column 4, lines 50-56.]**

With respect to **independent claim 14**,

"A method of collision detection, comprising: detecting an address match between two or more ports; **[Luo teaches this limitation, e.g. in column 4, lines 50-56]** *and generating a collision flag* **["WAIT STATE"]** *for at least one of the two or more ports of any of the other of the two or more ports are writing, the collision flag providing an indication that at least one of the two or more ports may have read or written corrupted data."* **[Luo discloses in column 4, lines 57-61, "The asynchronous, simultaneous access wait state generator 123 generates a wait state signal WAIT STATE 1 relating to the first port of the dual port device, and a wait state signal WAIT STATE 2 relating to access from the second port of the dual port device. " Luo teaches this limitation, e.g. in column 4, lines 50-56.]**

Dependent Claims

With respect to **claim 2**,

"The system of claim 1, further including control logic coupled to the memory array **[disclosed, e.g. in FIG. 1 and column 1, lines 23-26]** *to receive signals associated with the at least two ports* **[Luo discloses in the abstract, "dual port device"]** *and present signals to the memory array."* **[Luo discloses this limitation, e.g. in the abstract, "a wait state signal is generated for the relevant port having the later attempt to access the same memory or other addressable location."]**

With respect to **claim 3**,

"The system of claim 1, wherein the collision detect circuit sets the collision flag associated with one of the at least two ports if another of the at least two ports is executing a write operation to a memory location at the same that that the one of the at least two ports accesses the memory location." **[Luo discloses in column 4, line 67 – column 5, lines 1-5, "...when the two simultaneous addresses are the same, and at least one of the operations is a write access, an access collision occurs. In such a case, a wait state signal is preferably generated to halt one of the processors or other addressing devices communicating with the respective ports of the dual port device."]**

With respect to **claim 4**,

"The system of claim 1, wherein the collision detect circuit comprises: an address compare circuit coupled to receive and compare addresses from each of the at least two ports and provide a match signals indicating which of the addresses are the same; **[Luo teaches this limitation, e.g. in column 4, lines 50-56, "If the two simultaneous addresses indicate a collision would occur in an access to the same address location, a same location signal SAME_LOC is activated, e.g., goes to a logic HIGH state for the duration of the collision of address signals. Otherwise, the same location signal SAME_LOC remains inactive, e.g., at a logic LOW state."]** *and at least one collision detect logic coupled to receive the match signals and the read/write signals and provide a collision signal for a first port of the at least two ports if the match signals indicate an address match between the first port and a second port of the at least two ports and the read/write signal associated with the second port indicates a write*

operation; **[Luo discloses in column 4, lines 57-61, "The asynchronous, simultaneous access wait state generator 123 generates a wait state signal WAIT STATE 1 relating to the first port of the dual port device, and a wait state signal WAIT STATE 2 relating to access from the second port of the dual port device. "]** *and at least one collision flag set circuit coupled to receive a collision signal from the collision detect logic* **["wait state generator 123"]***and set a collision detect flag according to the clock signal associated with the first port."* **[Luo discloses in column 5, lines 20-25, "...when a clock signal is at a logic HIGH), and the data is transferred, e.g., during the subsequent phase(0) (e.g., when the clock signal is at a logic LOW). Thus, when a collision is determined by the simultaneous access determination module 120 (e.g., when the same location SAME_LOC signal is activated)..."]**

With respect to **claim 5**,

"The system of claim 4, wherein the collision flag set circuit associated with the first port comprises: a flip-flop circuit that is set according to the collision detect flag; **[FIG. 4 and associated text e.g.]** *a first latch that latches an output signal from the flip-flop circuit on a rising edge of the clock signal associated with the first port; a second latch that latches a signal from the first latch* **["The first meta-stable wait state generator circuit 397 includes a meta-stable D-type Flip-Flop 310a (DFF), and the second meta-stable wait state generator circuit 399 includes another meta-stable DFF 310b." The examiner interprets a D Flip Flop as analogous to a latch. See FIGs. 3-4]** *on a falling edge of the clock signal associated with the first port;* **[Luo discloses in column 5, lines 20-25, "...when a clock signal is at a logic HIGH), and the data is transferred, e.g.,**

during the subsequent phase(0) (e.g., when the clock signal is at a logic LOW). Thus, when a collision is determined by the simultaneous access determination module 120 (e.g., when the same location SAME_LOC signal is activated)..."] *and an output driver coupled to receive a signal from the second latch and provide a collision detect flag."* **[FIG. 1, elements 110, 120, and 123]**

With respect to **claim 6**,

"The system of claim 5, wherein the flip-flop circuit is reset from the signal from the first latch." **[Luo discloses in column 6, lines 6-10, "The clear signal to the first meta-stable DFF 310a is provided by a NORed combination of the reset signal RESET and an ANDed combination of the WAIT STATE 1 and WAIT STATE 2 signals using a NOR gate 320 and an AND gate 330." See FIG. 4]**

With respect to **claim 7**,

"The system of claim 5, further including a first-in-first-out circuit to store addresses in response to the collision signal." **[This claim is taught by Luo in column 5, lines 15-30. Luo discloses that the circuit which maintains the WAIT STATE signals, utilizing the clock signal, can apply a particular accessing processor for retrieving addresses in the order in which it is received. The signals are stored in the circuit.]**

With respect to **claim 9**,

"The system of claim 8, wherein the collision detect circuit includes an address compare circuit **[FIG. 1, elements 110, 120, and 123]** *that provides a match signal when the left port address and the right port address are the same;* **[Luo teaches this limitation, e.g. in column 4, lines 50-56, "If the two simultaneous addresses indicate a collision would occur in an access to the same address location, a same location signal SAME_LOC is activated, e.g., goes to a logic HIGH state for the duration of the collision of address signals. Otherwise, the same location signal SAME_LOC remains inactive, e.g., at a logic LOW state."]** *a left port collision detect circuit that provides a left port collision signal when the match signal exists and when the right port is writing;* **[FIG. 1, elements 110, 120, and 123]** *a left port flip-flop that is set on the left port collision signal;* **[FIG.4 and associated text e.g.]** *a first left port latch that latches a collision flag from the left port flip-flop on a rising edge of a left port clock signal, wherein the left port flip-flop is reset according to the collision flag output from the first left port latch; a second left port latch that latches the collision flag from the first left port latch on a falling edge of the left port clock signal;* **[Luo discloses in column 5, lines 20-25, "...when a clock signal is at a logic HIGH), and the data is transferred, e.g., during the subsequent phase(0) (e.g., when the clock signal is at a logic LOW). Thus, when a collision is determined by the simultaneous access determination module 120 (e.g., when the same location SAME_LOC signal is activated)..."]** *and a left port output driver that provides the collision flag from the second left port latch."* **[FIG. 1, elements 110, 120, and 123] ["The first meta-stable wait state generator circuit 397 includes a meta-stable D-type Flip-Flop 310a (DFF),**

and the second meta-stable wait state generator circuit 399 includes another meta-stable DFF 310b." The examiner interprets a D Flip Flop as analogous to a latch. See FIGs. 3-4]

With respect to **claim 10**,

"The system of claim 9, further including a flip-flop **[FIG. 4]** *that stores the left port address* **[FIG. 3]** *according to the left port collision signal* **[e.g. FIG. 3, "WAIT STATE 2"].** *"* **[Luo discloses this limitation as shown in FIGs. 3 and 4. Luo discloses in column 3, lines 9-11, "FIG. 4 shows an exemplary D-type Flip-Flop synchronizer capable of resolving meta-stable condition in the circuit shown in FIG. 3."]**

With respect to **claim 13**,

"The method of claim 12, further including providing arbitration when either the left port collision flag or the right port collision tag is set." **[Luo discloses this limitation, e.g. in column 1, line 60 – column 2, line 6]**

With respect to **claim 15**,

"A method of collision detection, further comprising: providing arbitration when the collision flag is set." **[Luo discloses this limitation, e.g. in column 1, line 60 – column 2, line 6]**

ARGUMENTS CONCERNING PRIOR ART REJECTION

1ST POINT OF ARGUMENT:

Applicant's arguments filed on 9/25/2006 have been fully considered but they are not persuasive. With respect to the arguments on page 6, paragraph 4 of the applicant's remarks (as well as the arguments with respect to claims 8, 11, and 14 found on pages 7-8 of the applicant's remarks), the examiner believes that the amended limitation "*the collision flag providing an indication that any of the at least two ports may have read or written corrupted data"* is an "intended use" which is not supported by the corresponding structure.

In response to applicant's argument that Luo fails to teach at least the added amended limitation, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. Therefore, the examiner is maintaining the 102(b) prior art rejection.

Furthermore the examiners rejection of the applicant's claimed "collision flag" (SAME_LOC) is maintained due the intended use of the amended claim. The examiner notes that the SAME_LOC signal of the prior art can be *intended* to accomplish the same limitation or claimed result.

REFERENCES CITED BYTHE EXAMINER

The examiner notes the following reference: Fetzer et al. (US PG PUB No. 20040148559) teaches in paragraph [0016], **"When data is read from the storage array, 102, data-out, 112, is applied to a parity decoder, 104. The parity decoder generates a parity value, 118. This parity value, 118 is compared with the parity value, 116, stored in parity storage, 106. If the values, 116 and 118, don't match, a signal, 120 is sent to memory control indicating data corruption may have occurred."**

CONCLUSION

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy

Patent Examiner
Art unit: 2189

Reginald G. Bragdon

Supervisory Patent Examiner
Technology Center 2100